



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,024	04/20/2004	Aaron Ferrucci	ALTRP112/A1251	5974
51501	7590	08/07/2007		
BEYER WEAVER LLP			EXAMINER	
ATTN: ALTERA			KERVEROS, JAMES C	
P.O. BOX 70250				ART UNIT
OAKLAND, CA 94612-0250				PAPER NUMBER
			2117	
				MAIL DATE
				DELIVERY MODE
			08/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/829,024	FERRUCCI ET AL.
	Examiner JAMES C. KERVEROS	Art Unit 2117

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 10 July 2007.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-14 and 16-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-14 and 16-30 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 20 April 2004 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application
- 6) Other: _____.

DETAILED ACTION

This is a FINAL Office Action in response to Amendment filed 7/10/2007.

Claim 15 is cancelled. Claims 1-14 and 16-30 are presently under examination and pending.

Response to Arguments

Applicant's arguments filed 7/10/2007 in the Amendment, with respect to claims 1-14 and 16-30, have been fully considered but they are not persuasive.

Applicant argues that Normoyle does not teach or suggest any delay introduced by a secondary or slave component when responding to a primary component request. According to Applicant's further arguments, Normoyle is believed to describe only primary component pseudo randomly delaying interrupts or non-pseudo randomly delaying responses.

In response to Applicant's arguments, the Examiner wishes to direct Applicant's attention to Figs. 9 and 10 of Normoyle, which illustrate a method carried out in connection with an apparatus, including (step 1500) a primary component (master device 1060) issuing an interrupt request (P_INT_REQ) to a secondary component (slave device 1070) through arbitration logic (system controller, SC 1180). If at (step 1530) the target, such as the slave is unable to receive the pending INT request, then the method proceeds to step 1640, where the SC issues a negative acknowledgment (NACK) to the master, and the SC drops the P--INT--REQ without passing it on to the slave. At step 1650, the master waits a random (or pseudorandom) period of time, and then proceeds to step 1500 to reissue the INT request.

Even though, the system controller SC issues a NACK, which triggers the pseudorandom time delay (step 1650), the NACK is initiated by the (slave device 1070), because the slave is unable to receive the pending INT request, due to its PINT--RQ (INT request input queue) being full, i.e. it has received the maximum number of INT requests allowed to it by the depth of its PINT--RQ queue without issuing a P--IAK.

Clearly, the delay is determined by the slave device and not by the master device as argued by the Applicant. The master device merely waits a random (or pseudorandom) period of time (step 1650) prior to reissue the INT request.

Also, it is clear from the Abstract, that the system controller determines whether the target (slave device) interrupt handler's input queue is full, and if not then it passes on the interrupt request and sends a positive acknowledgment to the interrupter. If the queue is full, then a negative acknowledgment (NACK) is sent, and the interrupter (master device) then waits a random period of time and sends the interrupt request again. Evidently, the slave device initiated the ACK and NACK signals, while the master device does not initiate the time delay but rather waits prior to reissuing the INT request.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-14 and 16-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Normoyle (US Patent 5,892,957) issued: April 6, 1999.

Regarding independent Claims 1, 13, 21, 28, Normoyle discloses a method and apparatus directed to interrupt handling in a uniprocessor or multiprocessor system, including multiple master devices (M1, M3..M3) and slave devices (S1 . . . S2), which are coupled via a system controller 75, Fig. 1A, in the same fashion as the system controller 70 is coupled to the master and slave(s) in Fig. 1, where the master devices correspond to the primary components, the slave devices correspond to the secondary components and the system controller 75 correspond to the arbitration logic, also shown in Figs. 9 and 10, the method and apparatus comprising:

Receiving a request (P_INT_REQ) at a secondary component (device 1070) coupled to a primary component (device 1060) through arbitration logic (system controller), where the request is characteristic of a primary component request (P_INT_REQ), flow chart of Fig. 10, which illustrates the method carried out in connection with the apparatus of Fig. 9, as follows:

An interrupt event begins with the issuance of an interrupt request (P_INT_REQ) by the master, as at step (box) 1500 in Fig. 10. The system controller (SC) receives the INT request (box 1510), and determines (box 1520) from field 1010 (target ID) the appropriate target for the interrupt. This is done by SC logic 1430, i.e. circuitry and/or software configured in a conventional manner for this purpose.

At box 1530, the SC 1180 determines by examining its counter 1460 whether the slave interface 1290 can accept an INT request.

If at box 1530 the target is unable to receive the pending INT request, then the method proceeds to step 1640. In this case, the SC issues a negative acknowledgment (commonly called a NACK, and identified in FIGS. 9 and 10 as S--INAK) to the master, and the SC drops the P--INT--REQ without passing it on to the slave. At step 1650, the master waits a random (or pseudorandom) period of time, and then proceeds to step 1500 to reissue the INT request.

Regarding Claim 13, the system controller of Normoyle, also, functions as an interconnection module, for communicating asynchronous interrupt events as from interrupting sources to interrupt handler targets across a packet-switched interconnection network. According to Normoyle, "the interconnection network may in general take the form of a number of different standard communication topologies that interconnect masters and slaves, such as a point-to-point link, a single bus or multiple buses, or switching fabrics. The interconnect may employ any of a number of conventional mechanisms for switching the transaction request to a slave using one or more signal paths, and the switching may be based either on the addressing information contained in the transaction request packet, or on another protocol not necessarily dependent on the contents of the request packet".

Regarding Claims 2, 3, 5, 6, 8-12, 14, 17, 19, 20, 22-24, 26, 27, 29, 30, Normoyle discloses the randomness of the period of time that the master waits before resending an INT request helps to prevent situations where a given interrupter repeatedly sends interrupts to another device, preventing the receiving device from sending its own interrupts, by causing it to delay its own interrupts to process incoming interrupts from

the first interrupter. In this application, "random" may be taken to mean, truly random or pseudorandom, i.e. random with certain predetermined constraints. Thus, the interrupter is caused to delay some random period of time, and in that period the second device gets a chance to clear the outstanding interrupt(s) and issue its own interrupt request.

Regarding Claim 7, with respect to claimed limitation "switching fabric", Normoyle discloses the interconnection network may in general take the form of a number of different standard communication topologies that interconnect masters and slaves, such as a point-to-point link, a single bus or multiple buses, or switching fabrics.

Regarding Claim 18, Normoyle discloses the system controller (SC) 1180 includes a counter 1420 for monitoring the number of transactions pending at an associated slave's input queue and a 1460 for monitoring the number of outstanding interrupt requests to the slave interface 1290. At step 1650, the master waits a random (or pseudorandom) period of time, then proceeds to step 1500 to reissue the INT request, 2 where the waiting time period may be implemented with the a counter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Regarding Claims 4, 16, 25, Normoyle does not explicitly disclose a Linear Feed Back Shift register (LFSR) as delay mechanism.

However, in analogous art, Malek (US 5,086,467) discloses a secure communication system including a pseudo-random sequence itself, which is ideally suited for determining both the duration and the inter-transmission delays by using the output of the LFSR to seed random variable generators, one of which may be used to select the duration of any dummy traffic transmission, and the other of which may be used to determine the inter-transmission delay, or time between transmissions, (see Malek, Summary of the Invention and Figure 3). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate an LFSR in the apparatus of Normoyle as taught by Malek, for the purpose of generating a pseudo-random delay, since an LFSR is ideally suited for determining time delays.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Date: 31 July 2007
Office Action: Final Rejection

Tel: (571) 272-3824, Fax: (571) 273-3824
U.S. Patent and Trademark Office
Alexandria, VA 22314.
Email: james.kerveros@uspto.gov

JAMES C KERVEROS
Primary Examiner
Art Unit 2117

JAMES C KERVEROS
PRIMARY EXAMINER

